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INNOVATION PARTNERS
540 UNIVERSITY DRIVE
SUITE 300
PALO ALTO, CA 94301

EXAMINER	
LEE, CHRISTOPHER E	

ART UNIT	PAPER NUMBER
2112	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/042,971	JACOBSON, VAN	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-31 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-31 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 07 January 2002 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

2. The disclosure is objected to because of the following informalities:

Substitute "he" in lines 21-22 on page 6 by --the--.

Substitute "176" in line 12 on page 9 by --178--.

Appropriate correction is required.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because

a) reference character "288" has been used to designate both PROC C FIFO and Dispatch Storage in Figs. 2B and 2D.

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because

b) they do not include the reference sign 236 mentioned in the description in line 17 on page 26, and

c) they include the reference signs 200, and 250-268 in Fig. 2A not mentioned in the description.

5. For the cases a) and b), corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application.

For the case c), corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application.

Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement

Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

6. Claims 1, 3, 11, 13, 21, and 23 are objected to because of the following informalities:

a) The claims 1, 11, and 21 recite the subject matter "the plurality of entities" in line 7 of the claim 7, in line 18 of the claim 11, and in line 11 of the claim 21, respectively. However, it has not been specifically clarified in the claims 1, 11, and 21, respectively. Therefore, the Examiner presumes that the term "the plurality of entities" could be considered as --a plurality of entities-- in light of the specification since it is not defined in the claims.

b) In the claims 3, 13, and 23, delete "and" in lines 6, 7, and 8, respectively.

c) The claim 11 recites the subject matter "the incoming communication interface output" in line 9. However, it has not been specifically clarified in the claim 11. Therefore, the Examiner presumes that the term "the incoming communication interface output" could be considered as --the incoming communication interface provider-- in light of the specification since it is not defined in the claims.

d) The claim 11 recites the subject matter "the first storage input/output" in lines 16-17. However, it has not been specifically clarified in the claim 11. Therefore, the Examiner presumes that the term "the first storage input/output" could be considered as --the first interface input/output-- in light of the specification since it is not defined in the claims.

e) Where the Applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*,

190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). In this case, the Applicant acts as his or her own lexicographer to specifically define terms "sinebusly" and "sineinterruptusly" in the written description in lines 2-8 on page 14. However, the Applicant uses slightly different terms "sinebusslessly" and "sineinterruptessly" in the claims 1, 11, and 21, respectively, even though the meanings of terms "sinebusslessly" and "sineinterruptessly" in the claims 1, 11, and 21 are the same that the meanings of terms "sinebusly" and "sineinterruptusly" in the written description in lines 2-8 on page 14, in light of the scope of the claimed invention, respectively. Therefore, the Examiner presumes the terms "sinebusslessly" and "sineinterruptessly" could be considered as --sinebusly-- and --sineinterruptusly--, respectively, since they are not particularly defined in the specification.

Appropriate corrections are required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claim 31 is rejected under 35 U.S.C. 102(e) as being anticipated by Oden [US 6,862,282 B1].

Referring to claim 31, Oden discloses a method of processing a communication (i.e., ordering packets; See col. 1, lines 9-11), comprising:

- receiving the communication (i.e., en-queuing incoming data packets into input control & input queue 12 in Fig. 1, actually, into ingress packet pointer queue 102 of Fig. 3; See col. 3, lines 13-30);

- storing the communication (i.e., data packet) first storage (i.e., scheduled pointer queue 304, free pointer queue 306, and complete pointer queue 308 in Fig. 2) accessible to a plurality of entities (i.e., processors 0...N 18a-18N in Fig. 2);
- providing (i.e., de-queuing) the communication (i.e., data packet) from the first storage (in fact, said scheduled pointer queue, free pointer queue, and complete pointer queue being coupled to a corresponding processor of said plurality of processors, and writing said data packets to a plurality of processors 0...N 18a-18N in Fig. 2; See col. 4, lines 38-52);
- receiving a response to the communication (i.e., collector module 20 having an input for receiving complete packet pointer from pointer queues of a selected processor 18 in Fig. 3; See col. 5, lines 5-19);
- storing the response to the communication (i.e., data packet) in a second storage (i.e., ordering buffer 26 of Fig. 3) not accessible by at least one of the entities in the plurality of entities (i.e., collector module 20 is coupled to the selected packet processor, e.g., processor N, in Fig. 3, which means that said collector module is coupled to at least one of the plurality of processors but not coupled to unselected processors, and thus those unselected processors are not accessible by said unselected processors; See col. 5, lines 5-11); and
- providing the response from the second storage (i.e., de-queuing data packets from said ordering buffer 26 in Fig. 4).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-3, 5-7, 10-13, 15-17, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oden [US 6,862,282 B1] in view of Muller et al. [US 6,650,640 B1; hereinafter Muller].

Referring to claim 1, Oden discloses a method of processing a communication (i.e., ordering packets; See col. 1, lines 9-11), comprising:

- receiving the communication (i.e., en-queuing incoming data packets into input control & input queue 12 in Fig. 1, actually, into ingress packet pointer queue 102 of Fig. 3; See col. 3, lines 13-30);
- storing the communication received (i.e., en-queuing said ingress packet pointers of said incoming data packets into scheduled pointer queue 304, free pointer queue 306, and complete pointer queue 308 in Fig. 2);
- providing the communication stored (i.e., data packet) to at least one of a plurality of entities (i.e., writing said data packets to a plurality of processors 0...N 18a-18N in Fig. 2);
- receiving a response to the communication (i.e., collector module 20 having an input for receiving complete packet pointer from pointer queues of a selected processor 18 in Fig. 3; See col. 5, lines 5-19);
- storing the response (i.e., storing de-queued data packet into ordering buffer 26, which is shown as arrow 229 in Fig. 3; See col. 5, lines 20-29); and
- providing the response directly and sineinterruptusly (i.e., ordering module 22 operates walks said ordering buffer in sequence without using interrupt mechanism; See col. 5, lines 30-53).

Oden does not expressly teach that the storing operation for the communication received is directly and sinebusly performed.

Muller discloses a method for managing a network flow (See Abstract), wherein a feature of direct memory access mechanism (i.e., DMA engine 120 of Fig. 10) comprising

- storing a communication received (i.e., packet) directly and sinebusly (i.e., using direct memory access mechanism; See col. 9, line 66 through col. 10, line 1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said feature of direct memory access mechanism (i.e., DMA engine), as disclosed by Muller, in said method step of storing the communication received, as disclosed by Oden, for the advantage of providing the re-assembling feature for data portions of related packets, and thus the data can be more efficiently transferred to a destination entity through "page-flipping" (See Muller, col. 10, lines 42-56).

Referring to claim 2, Oden teaches

- the communication (i.e., data packet) is stored in a first storage (i.e., scheduled pointer queue 304, free pointer queue 306, and complete pointer queue 308 in Fig. 2) accessible to a plurality of entities (i.e., processors 0...N 18a-18N in Fig. 2);
- the response is stored in a second storage (i.e., ordering buffer 26 of Fig. 3) not accessible by at least one of the entities in the plurality of entities (i.e., collector module 20 is coupled to the selected packet processor, e.g., processor N, in Fig. 3, which means that said collector module is coupled to at least one of the plurality of processors but not coupled to unselected processors, and thus those unselected processors are not accessible by said unselected processors; See col. 5, lines 5-11); and
- the response is provided from the second storage (i.e., ordering module 22 de-queuing data packets from said ordering buffer 26 in Fig. 4).

Referring to claim 3, Oden teaches

- assigning (i.e., which means de-queuing to selected processor by distributor module 16 in Fig. 2; See col. 4, lines 25-38) the communication received (i.e., incoming data packets) to at least one of a plurality of queues (i.e., each processor having one set of scheduled pointer queue 304, free pointer queue 306, and complete pointer queue 308 in Figs. 2-4; in fact, said incoming data packets are en-queued, viz., being assigned, into said scheduled pointer queue 304, as indicated by path 215 in Fig. 2) in the first storage (i.e., said scheduled, free and complete pointer queues for all of processors 0...N 18a...18N in Figs. 2-4), the plurality of queues each (i.e., one set of scheduled pointer queue, free pointer queue, and complete pointer queue) corresponding to a different one of the entities (i.e., each queue set corresponds to each processor in Figs. 2-4); and
    - wherein the providing the communication step (i.e., being performed by said distributor module) comprises providing the communication (i.e., data packets) by to at least one of the plurality of entities corresponding to the at least one queue to which the communication was assigned (See col. 4, lines 39-62).

Referring to claim 5, Oden teaches

- assigning step is responsive to information contained in the communication (See col. 4, lines 35-38; i.e., wherein in fact that the distributor module selects one of the packet processors based on load balancing as determined from the load balancing module implies that assigning step (i.e., de-queuing step from input packet pointer queue) is the communication (i.e., data packets) responsive to information contained in the communication (i.e., based on the load status of current data packet)).

Referring to claim 6, Oden teaches

- the response is provided sinebusly (i.e., ordering module 22 operates walks said ordering buffer in sequence without using system memory bus for a plurality of processors 0...N 18a-18N in Fig. 4; See col. 5, lines 30-53).

Referring to claim 7, Oden teaches

- the communication (i.e., data packet) comprises a packet (See col. 3, lines 17-18).

Referring to claim 10, Oden teaches

- the plurality of entities (i.e., processors 0...N 18a-18N in Fig. 2) comprise a plurality of processors (See col. 3, lines 31-38).

Referring to claim 11, Oden discloses a system (i.e., data processing system) for processing a communication (i.e., ordering packets; See col. 1, lines 9-11), comprising:

- an incoming communication interface (i.e., POS-PHY physical layer interface for network processor in Fig 1) having an input (i.e., interfacing port of said physical layer interface for incoming data packets from input device 2 in Fig. 1) for receiving the communication (See col. 3, lines 13-30),
    - the incoming communication interface (i.e., said POS-PHY physical layer interface for network processor) for providing at least a portion of the communication received at the incoming communication interface input (i.e., said incoming data packets are provided to input control & input queue module 12 in Fig. 1; See col. 3, lines 18-19, wherein in fact that said network processor processes said incoming data packets inherently anticipates the incoming communication interface for providing at least a portion of the communication received at the incoming communication interface input);

- an incoming interface manager (i.e., input control & input queue module 12 of Fig. 1) having an input (i.e., ingress packet pointer queue 102 of Fig. 2) coupled to the incoming communication interface provider (in fact, said ingress packet pointer queue being coupled to the inward arrow from said POS-PHY physical layer interface for network processor to said input control & input queue module),
    - the incoming interface manager (i.e., said input control & input queue module) for storing the communication received (i.e., en-queuing data packets) at the incoming interface manager input (i.e., at said ingress packet pointer queue) into a first storage (i.e., scheduled pointer queue 304, free pointer queue 306, and complete pointer queue 308 in Fig. 2) coupled to an output (i.e., coupled to an output from/to distributor 16 in Fig. 2);
- a first interface (i.e., distributor module 16 of Fig. 2) having an input/output coupled to the first storage (i.e., said distributor module having an input/output to said pointer queues in Fig. 2) and an output (i.e., an output to processor packet memory 302 in Fig. 2),
    - the first interface (i.e., said distributor module) for retrieving (i.e., de-queuing) from the first storage via the first interface input/output and for providing via an output the communication to at least one of a plurality of entities (i.e., writing said data packets to a plurality of processors 0...N 18a-18N in Fig. 2) coupled to the first storage output (in fact, said scheduled pointer queue, free pointer queue, and complete pointer queue being coupled to a corresponding processor of said plurality of processors in Fig. 2; See col. 4, lines 38-52);
- a second interface (i.e., collector module 20 of Fig. 2) having an input for receiving a response to the communication (i.e., said collector module having an input for receiving complete packet pointer from said pointer queues in Fig. 3) and for providing (i.e., de-queuing) the response to a second storage (i.e., ordering buffer 26 of Fig. 3) coupled to an output (i.e., said ordering buffer is

coupled to an output from said collector module, which is shown as arrow 229 in Fig. 3; See col. 5, lines 5-29); and

- an outgoing interface manager (i.e., output control & output queue module 24 of Fig. 1) having an input/output coupled to the second storage (i.e., said output control & output queue module having an input/output, from ordering module 22, and to output device 4, which is coupled to said ordering buffer 26 in Fig. 1),
    - the outgoing interface manager (i.e., said output control & output queue module) for retrieving (i.e., reading from said ordering buffer) the response directly and sineinterruptusly (i.e., ordering module operates walks said ordering buffer in sequence without using interrupt mechanism) from the second storage and providing the response at an output (See col. 5, lines 30-53).

Oden does not expressly teach that the storing operation is directly and sinebusly performed to the first storage.

Muller discloses an apparatus for managing a network flow (See Abstract), wherein a direct memory access mechanism (i.e., DMA engine 120 of Fig. 10) comprising

- an incoming interface manager (i.e., DMA manager 1002 of Fig. 10) stores a communication (i.e., packet) received at an incoming interface manager input (i.e., an input from packet queue 116 in Fig. 10) directly and sinebusly (i.e., using direct memory access mechanism) into a first storage (i.e., processor memory page; See col. 9, line 66 through col. 10, line 1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said direct memory access mechanism (i.e., DMA engine), as disclosed by Muller, in said incoming interface manager (i.e., input control & input queue module), as disclosed by Oden, for the advantage of providing the re-assembling feature for data portions of related packets, and thus the data

can be more efficiently transferred to a destination entity through "page-flipping" (See Muller, col. 10, lines 42-56).

Referring to claim 12, Oden teaches

- the first storage output (i.e., an output from pointer queues, viz., scheduled pointer queue 304, free pointer queue 306, and complete pointer queue 308 in Fig. 2) is coupled to a plurality of entities (i.e., said output from pointer queues is internally couple to a plurality of processors 0...N 18a-18N in Fig. 2); and
- the second interface input (i.e., collector module 20 having an input for receiving complete packet pointer from said pointer queues in Fig. 3) coupled to at least one of the plurality of entities but coupled to fewer than all of the plurality of entities (i.e., said collector module is coupled to the selected packet processor, e.g., processor N in Fig. 3, which means that said collector module is coupled to at least one of the plurality of processors but coupled to fewer than all of the plurality of processors; See col. 5, lines 5-11).

Referring to claim 13, Oden teaches

- the incoming interface manager (i.e., input control & input queue module 12 of Fig. 1) is additionally for assigning (i.e., which means de-queuing to selected processor by distributor module; See col. 4, lines 25-38) the communication received (i.e., incoming data packets) to at least one of a plurality of queues (i.e., each processor having one set of scheduled pointer queue 304, free pointer queue 306, and complete pointer queue 308 in Figs. 2-4; in fact, said incoming data packets are en-queued, viz., being assigned, into said scheduled pointer queue 304, as indicated by path 215 in Fig. 2) in the first storage (i.e., said scheduled, free and complete pointer queues for all of processors 0...N 18a...18N in Figs. 2-4), the plurality of queues each (i.e., one

set of scheduled pointer queue, free pointer queue, and complete pointer queue) corresponding to a different one of the entities (i.e., each queue set corresponds to each processor in Figs. 2-4); and

- wherein the first interface (i.e., distributor module 16 of Fig. 2) provides the communication (i.e., data packets) by to at least one of the plurality of entities corresponding to the at least one queue to which the communication was assigned (See col. 4, lines 39-62).

Referring to claim 15, Oden teaches

- the incoming interface manager (i.e., input control & input queue module 12 of Fig. 1) assigns the communication responsive to information contained in the communication (See col. 4, lines 35-38; i.e., wherein in fact that the distributor module selects one of the packet processors based on load balancing as determined from the load balancing module implies that the incoming interface manager (i.e., said input control & input queue module) assigns (i.e., de-queues from input packet pointer queue) the communication (i.e., data packets) responsive to information contained in the communication (i.e., based on the load status of current data packet)).

Referring to claim 16, Oden teaches

- the outgoing interface manager (i.e., output control & output queue module 24 of Fig. 1) additionally retrieves the response from the second storage (i.e., reading data packet from ordering buffer 26 in Fig. 4) sinebusly (i.e., ordering module 22 operates walks said ordering buffer in sequence without using system memory bus for a plurality of processors 0...N 18a-18N in Fig. 4; See col. 5, lines 30-53).

Referring to claim 17, Oden teaches

- the communication (i.e., data packet) comprises a packet (See col. 3, lines 17-18).

Referring to claim 20, Oden teaches

- the plurality of entities (i.e., processors 0...N 18a-18N in Fig. 2) comprise a plurality of processors (See col. 3, lines 31-38).

11. Claims 4 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oden [US 6,862,282 B1] in view of Muller [US 6,650,640 B1] as applied to claims 1-3, 5-7, 10-13, 15-17, and 20 above, and further in view of Kimball et al. [US 6,345,041 B1; hereinafter Kimball].

Referring to claim 4, Oden, as modified by Muller, discloses all the limitations of the claim 4, including the assigning step is responsive to the load status of current communication (i.e., load balance information; See Oden, col. 4, lines 35-38, wherein, in fact the distributor module selects one of the packet processors based on load balancing as determined from the load balancing module implies that the assigning step (i.e., de-queuing step from input packet pointer queue) is the communication (i.e., data packets) responsive to the load status of current communication (i.e., based on the load status of current data packet)), except that does not expressly teach the assigning step is responsive to a prior communication.

Kimball discloses a method for automatic load-balancing on multisegment devices (See Abstract), wherein

- an undo prior load-balancing process (See col. 9, lines 17+) takes information responsive to a prior communication (i.e., responsive to the stored information at a prior load-balancing activation; See col. 9, lines 34-38).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included a feature of said automatic load-balancing, as disclosed by Kimball, in said

method, as disclosed by Oden, as modified by Muller, for the advantage of providing automatic determination of when a given said assigning operation by said incoming interface manager (i.e., load balancing activation by user) would not be beneficial, thereby keeping said system (i.e., the user's network) from being unnecessarily disturbed when no real beneficial would be gained (See Kimball, col. 9, lines 39-49).

Referring to claim 14, Oden, as modified by Muller, discloses all the limitations of the claim 14, including the incoming interface manager (i.e., input control & input queue module 12 of Fig. 1; Oden) assigns the communication responsive to the load status of current communication (i.e., load balance information; See Oden, col. 4, lines 35-38, wherein, in fact the distributor module selects one of the packet processors based on load balancing as determined from the load balancing module implies that the incoming interface manager (i.e., said input control & input queue module) assigns (i.e., de-queues from input packet pointer queue) the communication (i.e., data packets) responsive to the load status of current communication (i.e., based on the load status of current data packet)), except that does not expressly teach the incoming interface manager assigns the communication responsive to a prior communication.

Kimball discloses an apparatus for automatic load-balancing on multisegment devices (See Abstract), wherein

- an undo prior load-balancing process (See col. 9, lines 17+) takes information responsive to a prior communication (i.e., responsive to the stored information at a prior load-balancing activation; See col. 9, lines 34-38).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included a feature of said automatic load-balancing, as disclosed by Kimball, in said system (i.e., data processing system), as disclosed by Oden, as modified by Muller, for the advantage of providing automatic determination of when a given said assigning operation by said incoming interface

manager (i.e., load balancing activation by user) would not be beneficial, thereby keeping said system (i.e., the user's network) from being unnecessarily disturbed when no real beneficial would be gained (See Kimball, col. 9, lines 39-49).

12. Claims 8, 9, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oden [US 6,862,282 B1] in view of Muller [US 6,650,640 B1] as applied to claims 1-3, 5-7, 10-13, 15-17, and 20 above, and further in view of Wilson et al. [US 6,738,821 B1; hereinafter Wilson].

Referring to claims 8 and 9, Oden, as modified by Muller, discloses all the limitations of the claims 8 and 9, respectively, except that does not expressly teach the communication comprises an Ethernet frame and a storage device communication.

Wilson discloses an Ethernet storage protocol networks (e.g., cluster server system 103 in Fig. 1C), wherein

- a communication (i.e., data packet traffic in an ESP network; See col. 7, lines 2-16) comprises an Ethernet frame (i.e., Ethernet standards; See col. 7, lines 28-35) and a storage device communication (See col. 4, lines 43-62 and col. 9, line 63 through col. 10, line 8).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied said Ethernet storage protocol, as disclosed by Wilson, to said method, as disclosed by Oden, as modified by Muller, for the advantage of providing a simplification of the communication elements needed to transfer data over a network and enabling nearly unlimited scalability (See Wilson, col. 5, lines 11-15).

Referring to claims 18 and 19, Oden, as modified by Muller, discloses all the limitations of the claims 18 and 19, respectively, except that does not expressly teach the communication comprises an Ethernet frame and a storage device communication.

Wilson discloses an Ethernet storage protocol networks (e.g., cluster server system 103 in Fig. 1C), wherein

- a communication (i.e., data packet traffic in an ESP network; See col. 7, lines 2-16) comprises an Ethernet frame (i.e., Ethernet standards; See col. 7, lines 28-35) and a storage device communication (See col. 4, lines 43-62 and col. 9, line 63 through col. 10, line 8).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied said Ethernet storage protocol, as disclosed by Wilson, to said system (i.e., data processing system), as disclosed by Oden, as modified by Muller, for the advantage of providing a simplification of the communication elements needed to transfer data over a network and enabling nearly unlimited scalability (See Wilson, col. 5, lines 11-15).

13. Claim 21-23, 25-27, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oden [US 6,862,282 B1] in view of Muller [US 6,650,640 B1] and what was well known in the art, as exemplified by Luo et al. [US 6,265,885 B1; hereinafter Luo].

Referring to claim 21, most of the claim limitations have already been discussed/addressed with respect to claim 1, with the exception of a computer program product comprising a computer useable medium having computer readable program code embodied therein for processing said communication, the computer program product comprising computer readable program code devices configured to cause at least one computer to performs said method steps of the claim 1 (e.g., storage device having a computer software program).

The Examiner takes Official Notice that said method in the claim 1 being implemented in a computer readable program (i.e., a computer software program), and being stored in a computer useable medium (i.e., storage device), is well known to one of ordinary skill in the art, as evidenced by Luo (See Claim 9, lines 2-4).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have implemented said method of the claim 1 in said computer readable program (i.e., a computer software program), and being stored in said computer useable medium (i.e., storage device) since it would have provided a better flexibility of implementing said method than a hardware implementation, such as an easy modification, etc.

Referring to claims 22, 23, 25-27, and 30, all of the claim limitations in each of the claims 22, 23, 25-27, and 30 have already been discussed/addressed with respect to each of the claims 2, 3, 5-7, and 10, respectively.

14. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oden [US 6,862,282 B1] in view of Muller [US 6,650,640 B1] and what was well known in the art, as exemplified by Luo [US 6,265,885 B1] as applied to claims 21-23, 25-27, and 30 above, and further in view of Kimball [US 6,345,041 B1].

Referring to claim 24, all of the claim limitations in the claim 24 have already been discussed/addressed with respect to the claim 4.

15. Claim 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oden [US 6,862,282 B1] in view of Muller [US 6,650,640 B1] and what was well known in the art, as exemplified by Luo [US 6,265,885 B1] as applied to claims 21-23, 25-27, and 30 above, and further in view of Wilson [US 6,738,821 B1].

Referring to claims 28 and 29, all of the claim limitations in each of the claims 28 and 29 have already been discussed/addressed with respect to each of the claims 8 and 9, respectively.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Evans et al. [US 6,253,250 B1] disclose method and apparatus for bridging a plurality of buses and handling of an exception event to provide bus isolation.

Hoffman et al. [US 6,094,435 A] disclose system and method for a quality of service in a multi-layer network element.

Port et al. [US 5,406,322 A] disclose packet-switched ring network having direct access to low and high bandwidth method.

Bass et al. [US 6,862,292 B1] disclose method and system for network processor scheduling outputs based on multiple calendars.

Broberg, III et al. [US 6,453,366 B1] disclose method and apparatus for direct memory access (DMA) with dataflow blocking for users.

Ben Num et al. [US 6,928,482 B1] disclose method and apparatus for scalable process flow load balance of a multiplicity of parallel packet processors in a digital communication network.

Minoru [JP 08-340348] discloses information processing system.

The Examiner refers to Minoru [JP 08-340348] reference as a prior art made of record and not relied upon the claim rejection(s) in the instant Office Action, and it is referred to the original copy of foreign reference in foreign language (i.e., Japanese). The Examiner attaches a machine translated copy of the reference for the convenience of the Applicant. However, the Examiner cautions the Applicant that the Office is not responsible for any erroneous interpretation resulting from inaccuracies between the original foreign language reference and the machine translation of the reference, as the machine translation may not reflect the original precisely.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher E. Lee
Examiner
Art Unit 2112

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